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Changing of the guard at IPC

A
ter many months of deliberation, IPC announced at the end of March, the new President to succeed Denny McGuirk and take the association forward into the next chapter. John W. Mitchell has an electronics background with Alpine Electronics and Bose Corporation, which makes a refreshing change to previous incumbents that came from outside of our industry.

New management in any organization also heralds changes and it was no surprise to see Mitchell bringing in Edward Trackman as VP of special projects to assist him with his mandate to grow the association internationally. Trackman worked alongside Mitchell in both his previous positions at Bose Corporation and more recently at Golden Key International Honour Society.

As part of this mini-reshuffle, Tony Hilvers has moved on to pursue other ventures. Tony served IPC well, but he established a number of entrenched positions from his many years within the industry. We wish him well in his new endeavors, but hope this will open up a new channel of rapprochement between IPC and other trade associations. The industry is too small and cost-conscious to afford feuding trade associations at the expense of the industry.

Markets continue to lag

We are by now well into the middle of the summer doldrums where everything slows down and manufacturing in some countries closes for the month of August. I have never understood how these countries can afford such a luxury. Germany, which was the biggest exponent seems to be making bigger efforts to keep the lights on this summer with more than just a skeleton staff to help keep their businesses running and trading.

However, the general picture is one of slow growth as many investment decisions are on hold during the current economic environment. One company that is certainly bucking that trend is MYDATA. See my interview on page 24 They have enjoyed two consecutive years of 30%+ growth, driven by an expanding mid-range, high-mix market and innovation.

Innovation and (dare I say it ) marketing is key during times like these as they sow the seeds for growth when the markets return to normal. You may not make as much from your new products as you would in the good times, but at least you are still selling products.

—Trevor Galbraith.
Looking to replace costly SAC305 solder paste with no- and low-silver alloys without sacrificing quality and reliability?

A virtual drop-in for SAC305, AIM’s new **NC259 Solder Paste** was designed specifically for alloys such as SN100C and SAC0307.

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www.aimsolder.com - info@aimsolder.com
When I was still quite new in this industry, aeroplanes had propellers and there was still an air of magic about PCB assembly, it was normal to work with local guys. Your boards came from “down the street” or at least the same region, with “better and cheaper” alternatives, some were.

A local distributor supplied all of things you needed, or at least the ones you had to. They were our “trusted advisors” but we never thought of them like that, they just helped us solve problems, most of the time, neither of us had seen before. Sticking components without leads onto a board with glue, then putting them through a solder wave really was exciting in the early days. Choices were limited from dispensing systems to materials; there were plenty of Wave Soldering systems, but many needed modifying for this “new technology”.

Solder Paste was the “next big thing” involving a complete redesign of the assembly process area; I did not say line as many did not have lines. Still we worked with the “local guy” but now probably supported by a technical expert. The partnership remained strong and if you had a process which was working, you thought really hard before you changed anything! It was a case of “if it ain’t broke, leave it the hell alone!”

Over time equipment and materials became more abundant and a lot of sales guys started knocking on doors and offering “better and cheaper” alternatives, some were telling the truth, some lied. But they were mostly rebuffed in the early days as you stuck with the guy who had helped and who, you knew, you could call on for help if something went wrong. The Partnership was still strong and working well for both sides.

However we then hit one of the many cyclical down turns in our industry and we were not ready. No one saw it coming and when it hit we were in poor shape to withstand it. So we looked to save money on materials, people, and advertising, anything which we could easily draw a line through or replace with a smaller number, to save a few bucks. Now we know we should have looked at waste, rework, production efficiency and many other positive responses, but we were new to this and scared. So almost overnight partnerships were destroyed, relationships built over many years severed for a “few dollars more”, or less in this case.

So we had new materials, different equipment and soon we found out that one of the reasons it was cheaper was the lack of support. We battled with this for a while, sometimes returning to our previous suppliers but at a lower price.

Then as we went up the next positive curve on the graph, we all became inundated with people trying to sell us something better and faster than what we had. Large companies soon realised that they had a big problem because techies and purchasing people were spending a lot of time, talking to these guys and trying their wares. So the Approved Vendor List was born, a team of senior guys chose partners to work with, excluding all others. A true case of “You’re not on the list, you’re not getting in!” When a good partner was chosen and this rule adhered to the system worked well, which was mainly the case in the early days. The companies got standardisation and the suppliers got continuity so invested in the relationship too.

But when the next downturn came, what did we do? Exactly the same as before, tried to save money by putting lines through stuff and writing smaller numbers on orders, we still had most of the same manufacturing inefficiencies but we never looked there. So the AVL and its associated price list came under immense pressure and the Partnership died once more. Killed for a few dollars less, but taking with it the extra support which long term relationships always almost build.

With an AVL just a price negotiation starting point, other companies doing similar things were added, so an AVL may contain 2 or 3 Reflow Oven manufacturers. So now there was simply a price battle to see who won the business, nothing about Partnership or Support. These may have been taken as “a given” but seldom were actually in the mix at the final price. This was simply due to suppliers having to cut to the bone to win orders.

If we are honest there are many companies doing this now as the whole industry shudders under the weight of Global downturn. However the enlightened ones are looking at reducing costs by improving efficiency and reducing waste and rework. There are a myriad of positive things that cut cost and improve the bottom line and actually would be good practice even in the “good times”.

The best way of doing this is working with the suppliers as partners, these times are tough for them too, efficiency reduces cost and over the last few years the OEM guys have become experts in this. From Smart storage to great utilisation software, from better syringes with less waste to brand new technologies, from PIHR to solder paste for low voiding. All these can add to the bottom line and actually increase the competitiveness of companies who work in this way.

So Partnerships are once more really making a difference in the marketplace, many companies are moving from the “lowest price” model to one which really gives them commercial and technical advantages. I have recently heard a couple of interesting comments. A very senior Procurement guy saying “I do not want an AVL or Agreement with you guys, I want us to work together to overcome challenges which new technology will bring and if you solve our problems we will buy your stuff”. Another similar level guy “Your system is not on our AVL but the AVL system does not do what we want, the system on our AVL is 5 years old and the other company do not have a newer suitable system. I do not want to add you to the AVL but want to work with you to ensure you get input from us into your roadmap”.

Sounds like Partnerships to me, none of them spoke about discount or price, but about making sure that both companies have strong links with each other. To take this full circle, I was told by an old guy a long time ago “The price of something is only a small part of its value or its cost”. Many millions have been lost in this industry just by buying cheap and now thankfully we are looking at the “value add” which a close working relationship with those around us brings to the table.
“Ease-of-Use Without Compromise”

If you are looking for fast programming, but don’t want to compromise on defect detection, MVP has the solutions to meet your business needs.

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While still providing enhanced measurement and defect detection techniques, MVP continues to invest, ensuring we can always provide the fastest programming times for our customers.
New Viscom representative in Scandinavia: CORE-emt A/S opens showroom in Denmark

CORE-emt A/S is the new Viscom representative for Denmark, Sweden and Norway. Steen Haugbølle, founder and head of CORE-emt, brings a great deal of experience in electronics manufacturing. He has already represented Viscom products for many years. In addition to Viscom, CORE-emt A/S also represents well-known products of all other significant production technologies.

Now CORE-emt has its showroom in Aars, Denmark—sufficient cause to also install an S3088 Viscom AOI system. Thus, customers and others with interest can now experience the inspection scope and working method of the Viscom AOI live. Alongside comprehensive advice, with his own CORE-emt service team Haugbølle also offers competent service and support for all Viscom products. www.viscom.com

PRIDE Industries places order for CyberOptics’ flagship 3-D SPI system – the SE500™

PRIDE Industries, Inc., a social enterprise providing first-rate manufacturing and service solutions to business and government, has purchased two SE500™ 3-D Solder Paste Inspection (SPI) systems for its manufacturing facility in Roseville, CA.

Designed to inspect the most demanding assemblies at >80 cm²/sec inspection speed without compromising measurement accuracy and repeatability. The SE500™ system provides PRIDE with a Dual Illumination sensor option to further improve repeatability and reproducibility on the very smallest of paste deposits.

Building on CyberOptics’ reputation as the provider of solder paste inspection systems with industry-leading volume accuracy, the SE500™ can inspect pad sizes down to 01005 component size (150 x 150 µm) while keeping up with ever-increasing line speeds. www.cyberoptics.com

ZESTRON augments its European Application Technology Team

ZESTRON, the global provider of precision cleaning products and services for the electronics manufacturing industry, has recently expanded its Application Technology Team.

In his role as Process Engineer, Mr. Wade is mainly responsible for key account support and customer care in Norway, Sweden, Finland, Denmark, the UK and Estonia. He supports his customers with finding new cleaning applications, performs on-site process optimizations and assists with process monitoring. www.zestron.com

Kyzen signs on leading rep firm in New England

Kyzen, a provider of environmentally responsible precision cleaning products for electronics and high-technology manufacturing operations, has signed on Matthew Associates as its manufacturers’ representative in New England. Matthew Associates has been serving all aspects of the electronics environment for more than 15 years in the New England area.

Matthew Associates will represent Kyzen’s line of environmentally responsible precision products and services throughout the New England territory. www.kyzen.com

Seika Machinery offers discount on McDry PCB storage cabinets to help customers meet IPC storage guidelines

Seika Machinery, Inc. revealed a special sale to assist its customers with meeting the IPC 1601 PCB Storage and Handling Guideline. Effective June 25-July 27, 2012, Seika Machinery is offering a special discount on McDry MC-1001 and MC-1002 PCB Storage Cabinets.
Juki wraps up 25k celebration with a strong presence at JISSO PROTEC

Juki Automation Systems recently participated in Juki’s 25,000th machine shipped celebration held in conjunction with the JISSO PROTEC 2012 exhibition, which took place June 13-15, 2012 at the Tokyo Big Sight in Japan. Juki saw record booth traffic during the three-day event as well as a great deal of interest in its new technologies.

Under the concept of 3E evolution: Easy, Economical, Expandable, Juki showcased cutting-edge products that improve productivity and quality.

New products displayed at the show for the first time included the TR-7D High-Speed Matrix Tray Server, MDS Matrix Tray Server, high-speed Sentry, and the KE-3010 high-speed chip shooter displayed together with the KE-3020V high-speed flexible mounter as one production line. Also of great interest at the show, the JX-100LED now offers the capability to handle board sizes up to 1200 mm. www.jukiamericas.com

Protec upgrades with MYDATA

To increase the flexibility, capacity and productivity of the SMT operations that are central to its manufacturing business, Protec Fire Protection plc, the UK’s largest privately owned fire detection company, has invested in two of MYDATA’s newest MY100DX14 pick-and-place machines. The machines are configured to work together in a Synergy arrangement and between them provide a total placement capacity of up to 80,000 cph.

Protec manufactures a wide range of electronic fire protection products, including fire detectors and control panels, and many of these products incorporate surface mount technology. Recently, however, the company’s existing SMT equipment was starting to show its limitations in terms of flexibility and capacity, and also it was no longer supported by its manufacturer.

Protec decided, therefore, to install a completely new SMT line that would not only satisfy its current requirements, but would also provide a dependable and flexible platform for future development and expansion. After carefully assessing the available options, the company made the decision to purchase its new pick-and-place machines from MYDATA.

One of the key factors that influenced the decision was the ability of the MYDATA machines to handle an exceptionally wide range of components, which would allow Protec’s designers to take full advantage of the latest developments in component technology.

Protec’s evaluation also showed that the Agilis feeders used by MYDATA are particularly easy to work with, and would facilitate the fast changeovers needed to achieve high productivity and profitability in the low volume, high mix environment that characterises the company’s manufacturing operations.

The final deciding factors were the quality of support provided by MYDATA, which has the largest dedicated SMT support team in the UK, and MYDATA’s proven stability as a company, since Protec was looking for equipment that it could rely on to underpin its growth well into the future.

The MYDATA Synergy line supplied to Protec can handle up to 352 x 8 mm feeders, making it suitable for use with even the most complex of products.

While the two MY100DX14 machines that make up the line normally work in combination support by sophisticated line-balancing software, they can also be used independently. This provides exceptional versatility allowing for example, each machine to handle a different product or one machine to continue operating while the other is taken out of service for replenishment or maintenance. www.mydata.com

LPKF: Record demand for laser systems for cutting printed circuit boards

The special mechanical engineering company LPKF reports a significant upswing in the demand for laser systems for cutting printed circuit boards. Incoming orders for this product line have already reached a level above EUR 10 million after only five months – sales of these products in the whole of the 2011 financial year were only around EUR 6 million. The clients include big-name international electronics groups.

“We continue to succeed on a regular basis in replacing conventional product methods with our laser technology,” says Dr. Ingo Bretthauer, CEO of LPKF AG. The UV laser cutting systems enable single printed circuit boards to be cut extremely precisely and in any shape from a larger multi-image board. The technology requires no mechanical tools or complex clamping systems. The cutting channel can also be right at the edge of the board because the high precision technology does not harm tracks or components.

With the system families LPKF MicroLine 6000 and LPKF MicroLine 1000, LPKF delivers concepts for industrial mass production, as well as production requiring very high variability. www.lpkf.com

Bob Murray oversees Eastern U.S. sales and service efforts for Acculogic, Inc.

Acculogic Inc., electronic production test solutions, announces that Bob Murray has joined the team as Eastern Regional Sales Manager. Murray brings more than 15 years of experience in increasingly responsible roles within marketing, sales and program management at several companies. In his most recent position, Bob was a program manager at Curtiss-Wright in New England.

Bob is based in Acculogic’s Woburn MA facility. As the company’s Regional Sales Manager, he is responsible for the overall sales and business development in the eastern United States and Canada. Bob will work closely with the product management and support teams to maintain existing customer relationships and build the company’s customer base. www.acculogic.com
Out on safari at ECTC

Sandra Winkler, Senior Industry Analyst, New Venture Research (newventureresearch.com), and IEEE/CPMT Luncheon Program Chair

San Diego, home to the world-famous San Diego Zoo and Wild Animal Park, also hosts the annual ECTC (Electronic Component Technology Conference) every three years. Attendance at this year’s 62nd ECTC was 1,230 people, who attended 347 presentations, up from 1,002 attendees the year prior. This was the second highest level of attendance since the inception of the ECTC 62 years ago. A total of 359 people attended the 16 professional courses on Tuesday, May 29th, and the conference boasted 81 exhibitors in the technology corner. The program sessions ran from May 30 through June 1, 2012. With so many people in attendance, there was a high level of energy in the air, with attendees on the hunt for new information. There was plenty of that to be found.

Additional sessions at various times provided even more information beyond that of the main conference sessions. A special session was held on Tuesday morning, titled “Next-Generation Packaging and Integration: The Transformed Role of the Packaging Foundry,” Chaired by Raj Pendse of STATS ChipPAC, speakers included Robert Lanzone of Amkor Technology, Bill Chen of Advanced Semiconductor Engineering (ASE), Mike Ma of Siliconware Precision Industries (SPI), Steve Anderson of STATS ChipPAC, and Dan Tracy of SEMI. Capital expenditures are going up by an order of a magnitude with TSVs in the equation, making it difficult for OSATs to fund their own growth. The need for collaboration was brought up not only here, but in many other conference sessions as well. About 3 percent of the top OSATs’ revenue is designated for R&D, which is feeding new technologies and helping these companies find new ways to reduce costs.

2.5-D is a hot topic, and is already in production in small quantities; bringing costs down will fuel the growth. TOs cost $35 in 1963 if the purchase price had not been artificially lowered (selling below cost), the industry would not have flourished as it did, when it did. The same will be true of other upcoming technologies—a lower cost will fuel purchasing power. The FOWLP, or fan-out wafer-level package, is opening up new possibilities of new markets. This technology can also enable a TSV stack; a dense interconnect silicon interposer will be needed for this.

In an effort to lower cost, many OSATs are moving to copper wire bonding, as the price of gold has become prohibitive. Because cost is such a strong underlying factor, the “high-end mentality” has to give way to trying the cheapest way first and building performance up from there. Producing something using the highest priced manufacturing technology makes it more difficult to reduce cost later.

The Tuesday night panel session, titled “Power Electronics—A Booming Market,” was chaired by Rolf Ashenbrenner of Fraunhofer IZM and Ricky Lee of Hong Kong University of Science and Technology. Speakers included Dan Kinzer of Fairchild Semiconductor, Klaus-Dieter Lang of Fraunhofer IZM, Lionel Cadix of Yole Development, Ljubisa Stevanovic of GE Global Research, and Bernd Roemer of Infineon Technologies AG. This technology is hot primarily in Europe, for renewable energies, power supplies, e-mobility, LED systems, smart power electronics, and network control. New materials and technologies will be needed in this market. Aluminum ribbon, copper aluminum ribbon, or copper wire bonding will replace aluminum wire bonding, and silver sintering or diffusion soldering for die attach will improve device life. The demand for power electronics is very regional.

The Wednesday morning Keynote speaker was Gregg Bartlett of GLOBALFOUNDRIES. He mentioned the need for collaboration during design, something that previously didn’t occur. This will bring the best minds to the table at the outset. 2.5-D and 3-D really require collaboration to make the whole fit seamlessly together. These technologies offer improved system-level performance and bandwidth with reduced latency and power requirements compared with competing technologies. 2.5-D and 3-D accommodate a smaller bump pitch. 2.5-D enables a “fission” of the CPU, GPU, and memory for high-bandwidth applications, integrating each chip individually into the whole so that each chip can have its own “needs” met, given that each involves different back-end processes. Silicon partitioning will occur with interposers, and increase with complexity, from FPGAs in 2011, memory cubes in 2013, and logic plus memory in 2013–2014 to, ultimately, wide-I/O memory on an application processor for more sophisticated heterogeneous stacking.

The Wednesday evening plenary session on “Photonics, Expanding Markets, and Emerging Technologies,” was chaired by Christopher Bower of Semприus, Inc. Speakers included Ashok Krishnamoorthy of Oracle, Jeff Perkins of Yole Development, Shen Liu of Huazhong University of Science and Technology, Alexander Fang of Aurrion, Timo Aalto of VTT Technical Research Centre of Finland, and Frank Libsch of IBM Corporation. LEDs, photonics integration on silicon, photonics packaging, and photonics to the processor chip were covered in this broad field.

Packaging is 40 percent of the cost of an LED, or light-emitting diode. The cell phone was the first killer application for LEDs; general lighting—otherwise known as HB (high brightness)—will be the next big thing for the LED market. Currently the cost of an LED light bulb is anywhere from $15 to $40 with rebates, compared with less than $1 for an incandescent bulb, putting LEDs out of reach for most residential customers. There are no standards for HB LEDs, and thermal issues are huge. The cost of an HB LED needs to come down by a factor of 10, which will come about with a lower-cost packaging solution, such as wafer-level packaging.

The photonics industry in general does not have much in the way of standards. Photonics involve using light to carry the
signal, rather than an electron. Photonics can be used in large-area data centers and on a single high-powered silicon chip. Uses abound in telecom, datacom, and computers. Because of the current high-cost manual processes to create photonic structures, efforts in recent years have focused on bringing costs down in a number of ways. In fiber-optic telecom uses, getting the package standardized, as in the IC world, has been up in the air for some time. Connecting the delicate fiber structures to a standardized package such as a butterfly package is difficult. The trick is to accomplish this without breaking the fiber-optic structures. Bringing photonics down to the computer level, either inter-chip or intra-chip, involves lowering the costs significantly by incorporating waveguides on silicon, a low-cost material. This is years away from actual production, and will require a killer application to justify spending the R&D costs to make it a reality. Germanium or some other material would have to be added to the mix, as silicon absorbs light, rather than reflects it, and the light cannot be absorbed if it is to continue carrying the signal down the line.

The final evening session on Thursday night was titled “Advanced Coreless Package Substrate and Material Technologies.” The co-chairs were Kishio Yokouchi of Fujitsu Interconnect Technologies and Venky Sundaram of Georgia Institute of Technology. Speakers included Yuji Nishitani of Sony Corporation, Tanaka Kuniyuki of Shinko Electric Industries Co., Takeshi Eriguchi of Asahi Glass Co., and Masateru Koide of Fujitsu Advanced Technologies.

Advantages of coreless substrates are several. Wiring capabilities allow direct signaling; all layers can be used as a signal layer. High performance comes from the lowest self-inductance and the highest mutual inductance. A coreless substrate is likely the widest bandwidth substrate structure.

Assembly problems include a higher warpage factor than with a cored substrate. Reflow is more difficult at higher temperatures. A number of options were presented to overcome warpage issues, including:

- Use of a clamp during chip attach
- Use of lower CTE insulator prepreg materials
- Use of a stiffener
- Lower temperature soldering

The program sessions ran for three full days, with six parallel sessions running at all times. Thus the topics to choose among were copious, and included advanced packaging methods such as 2.5-D/3-D, advanced interconnect, wafer-level packaging, LEDs, substrates, optoelectronics, modeling and simulation, materials and processing, RF, applied reliability, and emerging technologies. There was something for just about everyone connected to components, packaging, and manufacturing technologies (CPMT) in this jungle of options.
Conceived only after a Raytheon engineer noticed the effect of high-powered radar on his snack time chocolate bar, the microwave is a vivid illustration of how something designed for a specific purpose can have other, potentially more useful applications. And microwave-emitting radar sites are not alone in proving a catalyst for value elsewhere. SMT is getting in on the act too. But before we go into detail here, let's start at the beginning…with the print.

Anyone involved in stencil printing can attest to the personal frustration – not to mention the line inefficiencies – of having to constantly clean stencils. Particularly when printing small components, paste has a nasty habit of sticking in stencil apertures and/or contaminating the bottom of the stencil. Since some of these components are as little as 100 μm away from one another, any contamination or lack of precision in the printing process can lead to defects. And these defects – from insufficient solder, bridging, solder balls or flux residue – can mean you having to rework or scrap the PCB.

Up until now, the only way to deal with this was to frequently clean the stencil. In fact, with typical print cycle times lasting less than 20 seconds, and a 30-second cleaning cycle needed every two or three passes, it’s fair to say a significant amount of time is spent cleaning printers than printing with them.

Obviously, this costs a lot, both in wasted time and cost in cleaning consumables. So DEK took the decision to hit the problem head on. And this is where we bring the microwave back in; because, having spent time developing a solution, it turns out it can do an awful lot more than just save time and cut cleaning costs.

**Stencil coating breakthrough**

The product I’m referring to is Nano-ProTek, from DEK. And it is, we firmly believe, a breakthrough in stencil coating technology in that it overcomes many of the challenges in printing. In essence Nano-ProTek is a single-application agent that repels flux – and as a result we’ve termed it ‘fluxophobic’. That means it reduces solder paste’s tendency to stick to apertures and the bottom of stencils. It also helps under-stencil cleaning (USC) materials to do a better job, so the gasketing of the stencil to the PCB is improved.

To make sure it is not contaminating, we tested it with ion chromatography techniques and it passed the IPC 5704 standard
for cleanliness requirements for unpopulated printed boards, with all 13 ions under analysis well below the threshold for concern.

Crucially, Nano-ProTek is chemically inert when dry (so it does not interact with the paste) and is as safe as isopropyl alcohol to apply (all we recommend is using gloves in a ventilated area).

Customers and manufacturers alike can apply it in less than five minutes, with no need for specialized equipment. And it complies with European regulations on the Registration, Evaluation, Authorisation and Restriction of Chemicals (REACH), so you don't need to worry about hazardous waste disposal with it. Furthermore, it forms a permanent molecular bond so it is durable, lasting for thousands of cycles (unlike other coatings). However, unlike factory-only applied products, it can be reapplied at any time, whenever it is needed.

More than quick cleaning

Sounds good so far, right? But the best bit was when we started testing Nano-ProTek against conventional cleaning. First, as hoped, it greatly reduced the number of times you need to clean your stencils, easily by up to two to five times. In several cases it was even able to eliminate stencil cleaning completely. This in itself has a major impact on printer productivity and manufacturing efficiency, not to mention cutting the cost of consumables. However, there's more.

Customers that have started using Nano-ProTek have found that reducing the cleaning frequency considerably enhances the stability of their printing process.

With conventional cleaning cycles, the standard deviation for the print process is fairly large and only loosely clustered around a normal or Gaussian distribution. The number of defects per million opportunities (DPMO) is in the three figures, resulting in varying print volumes per run. Conversely, with Nano-ProTek, the standard deviation is much smaller and conforms much better to a normal distribution. This means the DPMO drops by an order of magnitude and print volumes are much more stable. Essentially, this amounts to an improvement in the process capability index (to 2.0 and above) and a progression from what is essentially a weak Six Sigma process to a strong Six Sigma. And this is achieved under conditions in which USC is needed every 30 prints, for example, instead of every three, resulting in a 36% higher throughput in terms of units per hour (UPH).

Reducing defects

It is commonly said that 50 per cent of defects can be traced back to the printing process, so anything that improves that process and makes it more stable is clearly desirable.

Indeed, it may be essential for the future of our industry. Right now, in terms of miniaturization, we are operating at the limits of our technological abilities and the only way to go further down in size is to perfect our processes to the nth degree. But you can't perfect a process that is out of control, say with a Cp close to or below 1.0. It is evident that Nano-ProTek gives us a way of stabilizing the print process so we can make further improvements in areas such as aperture design, paste type and stencil thickness.

Previously, attempting such improvements would have been considered a waste of time. And this potential for improvement applies to any manufacturing environment, be it high-volume, low-mix or low-volume, high-mix. Like the kitchen appliance that emerged from a chance encounter between a chocolate bar and a radar unit, the cleaning technology Nano-ProTek provides now enables us to tackle a whole new range of applications within SMT.

The proof's in the pasting

Meanwhile, the feedback so far about Nano-ProTek has all been overwhelmingly positive.

A company in the automotive sector reported that it had managed to do 106 prints without any under stencil cleaning and achieved a first-pass yield of 100 percent; a feat that was "not possible with stencils without Nano-ProTek." Another customer said that since it only printed batches of 40 to 50 units it had been able to dispense with under stencil cleaning altogether thanks to the product. An electronics manufacturing services (EMS) company told us: "After applying Nano-ProTek, the Cp is better, that means the printing becomes more stable. The yield is improved from 96.32 per cent to 99.39 percent. Based on the data we got, the influence on printing quality is positive even when changing the cleaning frequency."

One other EMS customer was even more forthright, though. It said: "Considering the printing quality, ROI analysis and UPH improvement, we suggest global deployment of this product on every stencil." Naturally, we couldn't agree more.
Drop test performance of BGA assembly using SAC105Ti solder sphere

Author: Weiping Liu, Dr. Ning-Cheng Lee, Simin Bagheri, Polina Snugovesky, Jason Bragg, Russell Brush, and Blake Harper.

Abstract
Board-level drop test performance was evaluated and compared for the following four different solder combinations in BGA/CSP assembly: 1) SnPb paste with SnPb balls, 2) SnPb paste with SAC105Ti balls, 3) SAC305 paste with SAC105Ti balls, and 4) SAC305 paste with SAC105 balls. The presence of Ti improved the drop test performance significantly, despite the voiding side effect caused by its oxidation tendency. It is anticipated that the voiding can be prevented with the development of a more oxidation-resistant flux. The consistently poor drop test performance of SAC105Ti/SnPb is caused by the wide pasty range resulting from mixing SAC105Ti with Sn63 solder paste. The effect of Ti in this system is overshadowed by the high voiding outcome due to this wide pasty range material. In view of this, the use of a SAC105 BGA with an SnPb solder paste is not recommended, with or without the Ti addition. Higher reflow temperatures drove the fracture to shift to the interface at the package side, presumably through building up the IMC thickness beyond the threshold value. A lower reflow temperature is recommended. The electrical response is consistent with the complete fracture data, but the complete fracture trend is inconsistent with that of the partial fracture trend, and neither data can provide a full understanding about the failure mode. By integrating the complete fracture and the partial fracture into a “Virtual Fracture”, the failure mechanism becomes obvious and data sets become consistent with each other.

Key Words: Drop test, lead-free solder, solder sphere, SAC, Ti, SAC105Ti, SAC105.

Introduction
Driven by environmental consideration, the electronics industry has been migrating toward lead-free soldering since the late 1990s. Presently, the prevailing solder alloys are mainly SnAgCu (SAC) alloys with high silver content, such as Sn3.8/Ag0.7/Cu (SAC387) and Sn3.0/Ag0.5/Cu (SAC305). Although high Ag SAC alloys are widely adopted, the fragility of the solder joints of array assembly packages, such as BGAs or CSPs, causes major concern for portable devices. Low Ag SAC alloys, such as SAC105, are proposed as a solution, but with only limited success. Other alloys, such as SAC alloys modified with a variety of additives, are also attempted. Again, the introduction driven by environmental consideration, the electronics industry has been migrating toward lead-free soldering since the late 1990s. Presently, the prevailing solder alloys are mainly SnAgCu (SAC) alloys with high silver content, such as Sn3.8/Ag0.7/Cu (SAC387) and Sn3.0/Ag0.5/Cu (SAC305). Although high Ag SAC alloys are widely adopted, the fragility of the solder joints of area array packages, such as BGAs or CSPs, causes major concern for portable devices. Low Ag SAC alloys, such as SAC105, are proposed as a solution, but with only limited success. Other alloys, such as SAC alloys modified with a variety of additives, are also attempted. Again, the outcome is mixed. Among those promising new materials, Ti has been reported as a very effective dopant to the SAC alloy for improvement of drop test performance in a simplified simulation study [1]. In this work, BGA solder spheres using SAC105 with a 0.02% addition of Ti (SAC105Ti) were evaluated for BGA assembly drop test performance. The results will be presented and discussed below.

Experimental
Materials
The following alloy combinations were tested in this work, as shown in Table 1. No-clean flux chemistry and type 3 powder were used for both Sn63 and SAC305 solder pastes.

<table>
<thead>
<tr>
<th>Set</th>
<th>Solder sphere</th>
<th>Solder paste</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sn63</td>
<td>Sn63</td>
</tr>
<tr>
<td>2</td>
<td>SAC105Ti</td>
<td>Sn63</td>
</tr>
<tr>
<td>3</td>
<td>SAC105Ti</td>
<td>SAC305</td>
</tr>
<tr>
<td>4</td>
<td>SAC105</td>
<td>SAC305</td>
</tr>
</tbody>
</table>

Table 1. Solder alloys used for solder sphere and solder paste.

Test Components
Three area array packages were used in this study, as shown in Table 2. In this work, SAC105Ti and SAC105 BGAs were made by reballing from previous SAC305 BGAs. Also, BGA256 is a perimeter array, while BGA196 is full array.

<table>
<thead>
<tr>
<th>Package</th>
<th>Body size</th>
<th>Sphere diameter (mm)</th>
<th>Pitch (mm)</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA256</td>
<td>27</td>
<td>0.76</td>
<td>1.27</td>
<td>2.56</td>
</tr>
<tr>
<td>BGA196</td>
<td>15</td>
<td>0.5</td>
<td>1.0</td>
<td>196</td>
</tr>
<tr>
<td>CSP64</td>
<td>8</td>
<td>0.46</td>
<td>0.8</td>
<td>64</td>
</tr>
</tbody>
</table>

Table 2. Area array packages used in this study.

Test Vehicle
The test vehicle is made of laminate poly-clad FR370HR material, 8” x 10” in size, with SMD pads and OSP surface finish. The board material has a Tg of 180°C and a decomposition temperature of 350°C, which provides tolerance toward lead-free reflow temperatures. Two components of each type were incorporated on the test
board, with a total of six components on each board, as shown in Figure 1.

**Test Matrix**
For the drop test, five boards were tested for each set of the four alloy combinations shown in Table 1. Overall, 20 boards were used for the drop test.

**Reflow Profile**
After solder paste printing and component placement, the board was reflowed with a 10-zone forced air convection oven under air. For the SAC305 paste assembly, profile 1 (Figure 2) was employed, with peak temperature 235+3°C, and 90±10 seconds above 217°C. For SnPb (Sn63) paste assembly, profile 2 (Figure 3) was employed, with peak temperature 230+3°C, and 60±10 seconds above 183°C.

**Drop Test**
This board-level drop test is based on the JEDEC Standard JESD22-B110A, known as the Subassembly Mechanical Shock Test. The shock parameters are 1500G, with 0.5ms duration. All cards were put through 100 drops, with one board tested at a time, and 20 boards in total. Two 220g weights were added to cards to increase strain and help induce solder failures. One board from each batch was monitored on two drops for shock input (with an accelerometer mounted to the board) and board strain. Each board was monitored in-situ for resistance changes. The first failure determined for each location was recorded as the number of drops to failure. If no failure was observed after 100 drops, the number was entered as 101.

**Dye and Pry Test**
After 100 drops were completed on all cards, the tested cards were immersed in red dye and subjected to a vacuum to force the dye into the pre-existing cracks caused by drop testing. The dye was then cured and the parts were pried off the board to inspect the failure modes.

**Results**

**Drop Test**

**BGA256**
The test results on BGA256 are tabulated in Table 3 for components located at corner (U204) and at edge (U205).

**BGA196**
The test results on BGA196 are tabulated in Table 4 for components located at corner (U206) and at edge (U207).

**CSP64**
The test results on CSP64 are tabulated in Table 5 for components located near corner (U208) and at edge (U209).

<table>
<thead>
<tr>
<th>Table 3. Drop test results for U204 and U205 (BGA256) locations.</th>
</tr>
</thead>
</table>

**Overall Average**
The average value of drop test performance shown in Table 3 to Table 5 is compiled in Table 6, with overall average calculated. The ranking of overall performance is: SnPb/SnPb ball (best) > SAC305/SAC105Ti ball > SAC305/SAC105 ball > SnPb/SAC105Ti ball.

<table>
<thead>
<tr>
<th>Table 6. Average of drop test performance.</th>
</tr>
</thead>
</table>

**Dye and Pry Test**
For the dye and pry test, the failures are categorized as complete fracture or partial fracture. Figure 4 shows the results of dye and pry test with complete fractures, while Figure 5 shows the results with partial fractures. All data presented is an average of 5 boards. When only a com-
Complete fracture is considered, as shown in Figure 4, the drop failure resistance ranking is: SnPb/SnPb ball (best) > SAC305/SAC105Ti ball > SAC305/SAC105 balls > SnPb/SAC105Ti ball. When only a partial fracture is considered, as shown in Figure 5, the drop failure resistance ranking is: SAC305/SAC105Ti ball (best) > SAC305/SAC105 ball > SnPb/SAC105Ti ball > SnPb/SnPb ball.

**Figure 4. Results of dye and pry test with complete fractures. Data presented is average of 5 boards.**

**Figure 5. Results of dye and pry test with partial fractures. Data presented is average of 5 boards.**

**Which Is Better? Electrical or Fracture Response**

Electrical Correlates with Complete Fracture The trend on the number of interconnects with complete fractures after 100 drops in each component and cell (Figure 4) matches the trend of electrical testing results in terms of the number of drops to first failure (Table 7). This close correlation reflects that the causes of the two failure types are fairly similar. Since electrical failure can only be caused by complete fracture, the mechanism which caused the first electrical failure, or first complete fracture, continued on causing more complete fractures after 100 drops. Alloy combinations, which are more prone to have a first complete fracture, also display more complete fractures after 100 drops.

Partial Fracture No Correlation The trend on the number of partial fractures on each component (Figure 5) does not match the trend of electrical drop testing results, since there was no change in electrical resistance, due to only partial interconnect failures.

**No Insight Out of Electrical**

By examining Table 7, the relative fracture resistance of alloy combinations varies with component type. No more electrical

---

**TABLE 7**

Table 7. Dye and pry test results on BGA256, BGA196, and CSP64.
test data is available for interpreting the significance of this component type sensitivity. This strongly suggests that electrical testing is not informative enough in understanding the effect of alloy combinations. Dye and pry tests may provide a deeper insight into the material performance.

**Combined Fracture Data Desired**

In the dye and pry test, a complete fracture does not reflect a partial fracture, including board cratering, thus is not representative of the potential of drop fracture resistance of alloy combinations. The fact that Figure 4 and Figure 5 exhibit different relative drop fracture resistance of alloy combinations indicates neither fracture mode can represent the potential of alloy combinations. Since both complete and partial fractures reflect damages associated with certain alloy combinations, the potential of alloy combinations toward drop fracture resistance should consider both fracture modes of the dye and pry test. Figure 6 shows the interconnect fracture modes defined in IPC/JEDEC-9702. Table 7 shows the crack sites determined in the dye and pry test on all area array packages tested. In this table, a partial crack is noted with an * on the site number associated.

**Integrating Fracture Data**

**Virtual Fracture**

Every individual complete fracture is assigned as "one" fracture. On the other hand, since partial fracture may range from nearly no fracture to nearly complete fracture, the median value 0.5 is adopted for every partial fracture. The total amount of the virtual fracture for each type of package/ alloy combination is the sum of complete fracture and partial fracture. For instance, a system with seven complete fractures and 10 partial fractures is regarded as having 7 + 10 x 0.5 = 12 virtual fractures.

**Normalizing Virtual Fracture**

In this study, 10 packages were analyzed for a dye and pry test for each package type and alloy combination. Table 8 shows the total number of solder joints tested in dye and pry tests for each system. For each system, the fracture is normalized by dividing the virtual fracture by the total number of joints tested. Table 9 shows the normalized virtual fracture of the systems studied. The fracture sites listed in Table 9 are illustrated in Figure 7.

**Failure Analysis**

**Effect of Package Size**

The size of the three packages is shown in Table 2, with the size decreasing in the order: BGA256 > BGA196 > CSP64. With all components located around the perimeter of the board, as shown in Figure 1, it is reasonable to expect the solder joint temperature of the packages at reflow to decrease in the following order: CSP64 > BGA196 > BGA256. This is evidenced by the observation that the microstructure of CSP64 is more uniform than BGA256 for 105Ti/SnPb paste system at the same oven setting, as shown in Figure 8.

**Effect of Pasty Range and Ti**

Excessive voiding was observed for both 105Ti/SnPb and 105Ti/305 solder joints, particularly in the case of 105Ti/SnPb. The excessive voiding associated with the assembly of SAC105 BGA with SnPb solder paste has been reported by Henshall et al. [2, 3], and was attributed to the 47°C wide pasty range (177°C to 224°C) of the alloy mixture. Since SAC105Ti is virtually identical with SAC105 in melting range [1], 105Ti/SnPb paste is also expected to have a similarly wide pasty range and the resultant excessive voiding. This excessive voiding caused by a wide pasty range is considered the root cause of an excessively
high fracture rate among all alloy combinations. In this case, the presence of Ti is estimated to have, at most, a minute effect. 105Ti/305 was observed to have more voiding than 105/305. This is attributed to the relatively high oxidation tendency of Ti, as illustrated by the Gibbs free energy of metal oxide formation of several metals at ambient condition [4], as shown in Table 11.

Table 11. Gibbs free energy of metal oxide formation at ambient temperature.

<table>
<thead>
<tr>
<th>Metal oxide</th>
<th>$\Delta G^\circ$ [kJ/mol]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MgO</td>
<td>-1220</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>-1150</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>-1040</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>-880</td>
</tr>
<tr>
<td>MnO</td>
<td>-805</td>
</tr>
<tr>
<td>SnO$_2$</td>
<td>-540</td>
</tr>
<tr>
<td>FeO</td>
<td>-480</td>
</tr>
<tr>
<td>NiO</td>
<td>-460</td>
</tr>
<tr>
<td>CuO</td>
<td>-300</td>
</tr>
</tbody>
</table>

Effect of Hot Reflow Temperature
As discussed in the previous section, a high reflow temperature drives the fracture site to shift from resin to solder interface. When the reflow temperature is high enough, such as the small package CSP64 with lead-free assembly, the fracture further shifts to the top of the interface of the solder joint, as shown in Figures 11 - 13. In general, the top interface went through two reflows, one for bumping, and one for assembly. On the other hand, the bottom interface went through one reflow only. It is hypothesized that at sufficiently high reflow temperatures, the IMC thickness at top interface exceeded a threshold value, thus becoming the primary fracture site. Here, presence of Ti appears to have a negligible effect. Table 13 summarizes the effect of hot reflow temperature on fracture site. Discussion The presence of Ti improved the drop test performance significantly, despite voiding side effect caused by its oxidation tendency. The flux used here is a regular no-clean flux. It is anticipated that the voiding can be prevented with the development of a more oxidation resistant flux. Once developed, the Ti-doped alloy is expected to have an even higher drop test performance.

Figure 10. Effect of alloy combination on fracture

However, despite this unfavorable effect of oxidation, 105Ti/305 still exhibits a lower overall fracture rate compared with 105/305, and is even lower than SnPb/SnPb for BGA256 and BGA196, as shown in Figure 10. The superior drop test performance of SACTi has been studied by Liu et al. [1] and is attributed to (1) the increased grain size and dendrite size, therefore reduced hardness of solder, (2) inclusion of Ti in the IMC layer, and (3) reduced IMC layer thickness. For CSP64, where the solder joint is considerably smaller and thus may be more sensitive to voiding, the voiding may dictate fracture performance. Table 12 summarizes the relation between pasty range and Ti on fracture performance.

Table 12. Effect of pasty range and Ti on fracture performance.

<table>
<thead>
<tr>
<th>Metal oxide</th>
<th>$\Delta G^\circ$ [kJ/mol]</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
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<tr>
<td>MnO</td>
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<tr>
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<td>NiO</td>
<td>-460</td>
</tr>
<tr>
<td>CuO</td>
<td>-300</td>
</tr>
</tbody>
</table>

Wide Pasty Range of Mixed Alloys
The consistently poor drop test performance of 105Ti/SnPb is caused by the wide pasty range resulting from mixing SAC105Ti with Sn63 solder paste. The effect of Ti in this system is overshadowed by the high voiding outcome due to this wide pasty range material. In view of this, the use of SAC105 BGA with SnPb solder paste is not recommended, with or without Ti addition.

Reflow Temperature
High reflow temperatures shifted the fracture site to the interface at the package side, presumably through building up the IMC thickness beyond the threshold value. A lower reflow temperature is recommended.

Virtual Fracture Model
The electrical response is consistent with the complete fracture data, but the complete fracture trend is inconsistent with that of the partial fracture trend, and neither data can provide a full understanding about the failure mode. By integrating the complete fracture and partial fracture into a "Virtual Fracture," the failure mechanism becomes obvious and the data sets become consistent with each other.

Table 13. Effect of hot reflow temperature on fracture site.

Conclusions
Board-level drop test performance was evaluated and compared with the following four different solder combinations in BGA/CSP assembly: (1) SnPb paste with SnPb balls, (2) SnPb paste with SAC105Ti
Drop test performance of BGA assembly using SAC105Ti solder sphere balls, (3) SAC305 paste with SAC105Ti balls, and (4) SAC305 paste with SAC105 balls. The Ti doping improved the drop test performance significantly, despite the voiding side effect caused by its oxidation tendency. It is anticipated that the voiding can be prevented with the development of a more oxidation resistant flux. The consistently poor drop test performance of 105Ti/SnPb is caused by the wide pasty range resulting from mixing SAC105Ti with Sn63 solder paste. The effect of Ti in this system is overshadowed by the high voiding outcome due to this wide pasty range material. In view of this, the use of a SAC105 BGA with an SnPb solder paste is not recommended, with or without the Ti addition. High reflow temperatures shifted the fracture site to the interface at the package side, presumably through building up the IMC thickness beyond the threshold value. A lower reflow temperature is recommended. The electrical response is consistent with the complete fracture data, but the complete fracture trend is inconsistent with that of the partial fracture trend, and neither data can provide a full understanding about the failure mode. By integrating the complete fracture and the partial fracture into a “Virtual Fracture,” the failure mechanism becomes obvious and data sets become consistent with one another.

Acknowledgement
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Dr. Ning-Cheng Lee, Vice President of Technology for Indium Corporation, is a world-renown soldering expert and an SMTA Member of Distinction. He has nearly 30 years of experience in the development of fluxes and solder pastes for SMT industries. He has extensive experience in the development of high temperature polymers, encapsulants for microelectronics, underfills, and adhesives. E-mail: nclee@indium.com Full biography:

References

First presented at APEX, 2012.
Electronic components used in the manufacture of electronic products are presently available in a wide variety of different sizes, shapes and formats. Electronic component catalogs are filled with page after page of offerings for both passive and active devices including both through hole and surface mount variations. JEDEC (Joint Electronic Device Engineering Council) under the aegis of its JC-11 committee oversees the registration of mechanical outlines of all electronic packaging. In the work of JC-11.11 which targets specifically micro-electronic plastic packages, there are more than 80 different standards for such packaging. Understanding the lexicon and terminology of standardized IC packaging can be quite challenging. Looking at just the matter of IC package thickness or package profile, one will find the following descriptions with their associated designators: low (L), thin (T), very thin (V), very very thin (W), ultra thin (U), extra thin (X1) and super thin (X2), paper thin (X3) and die thin (X4). Figure 1 provides a graphic to illustrate the differences. Interestingly, the same “80% rule” that was applied to lead pitch was adopted One must also keep in mind the different package and lead formats (BGA, CSP, DIP, FBGA, LGA, QFN, QFP, SIM, SIP, SOT, TSOP-1, TSOP-2, WLP, ZIP, etc.) with outlines identified for the different lead counts which can run from 3 to 3000 or more. There are as well, many different lead pitches (2.54, 1.27, 1.0, 0.8, 0.65, 0.5, 0.4, 0.3, 0.250 mm). Finally, there are also registered dual pitch components, dual lead type components and stackable components. It doesn’t take a background in mathematics to realize that the number of potential package variations can run into the many thousands.

There are a number of reasons for this situation. One key reason is that integrated circuit package designers must keep pace with the demands on the industry to make ever higher performing, lower cost, smaller/more compact and lighter weight electronic products and when it comes to designing electronic product, electronic components are the base on which the design must be build. However this does not address the fact that there are so many legacy components still being selected and used in electronic product designs. This seems to be indicative of the case that it may be very difficult for some designers and product developers to let go of the past. Once one becomes skilled at designing electronic assemblies with certain types of components is easy to default to the selection of such devices for any current design. We are after all creatures of habit. On the other hand some legacy components are very useful and well suited to the needs of hobbyists and independent product developers. Through hole leader devices, including dual in-line packages (DIP), pin grid arrays (PGA), transistor outline (TO cans), electrolytic capacitors and radial leaded discrete devices are much easier to work with manually than surface mount components when it comes to hand assembly. Many hobbyists are likely familiar with bread boards comprised of a piece of FR4 laminate perforated entirely with plated through holes all on 100 mil centers. Since nearly all dual in-line packages have their leads on 100 mil centers it makes it very easy for the hobbyist to place the components securely on the board and solder them into position, and then subsequently interconnect them to create an operational circuit using discrete wires soldered from point to point.

While the latter situation is understandable and even tolerable because it provides a means for the independent hobbyist, student or inventor to explore their ideas and build a base of understanding for the future, the wide variety of options ought not to be a necessity when it comes to designing and manufacturing electronic products if one sets about the task in a thoughtful way and exercises some discipline when choosing components for particular design. With that in mind we can return to a recurring theme which has been covered in this column over the years and that is the employment of a standard grid and the choosing of components whose terminations will fall on points within that standard grid. As has been mentioned before, there are significant advantages to doing so including the reduction of the number of layers required for routing which will reduce manufacturing cost. However, the
focus of this discussion is really on component thickness profile. And the somewhat rhetorical question remains the same: Do we really need that many different thicknesses? Returning to Figure 1 to consider again component thickness, as can be seen height is measured from the component lead seating plane (in the figure all components are shown as area array packages having solder balls for interconnection) to the top of the package. Obviously the contribution of the lead to overall component height will vary significantly from component format to component format with legacy products having a much higher profile than current generation devices. However note that the solder ball contributes almost half to the overall height of the component. Leadless devices such as QFNs and LGAs do not carry the burden of this extra height and thus can be lower profile, however when they are attached to the surface of a printed circuit board solder is still required and adds to the overall height of the component in the assembled form.

With all this in mind let’s return again to a topic which has been discussed in this column previously, solderless assembly for electronics or SAFE for short which is predicated on the Occam concept of minimalism in manufacturing electronic assembly. If one considers, without prejudice, the elimination of solder from the assembly process one should be able to see that one can not only reduce cost significantly but also increase reliability and performance. Moreover, if one makes thoughtful decisions relative to component type it should be possible to create an electronic assembly where all of the components are of a common thickness depending on availability of the desired type of IC in the desired packaging format of course. This has some significant advantages as one could, for example, build a substrate of aluminum were cavities are mechanically or chemically milled to a depth suitable to assure that all component leads are planar with the upper surface of the assembly making the buildup of interconnection layers a simple process. Figure 2 is provided to graphically illustrate both the concept and the potential. This topic will be revisited again in the future, filling in some additional detail relative to both the process and its potential.

![Figure 1. As illustrated above JEDEC mechanical outline standard for IC packaging dishes out an alphabet soup of designators to define various IC package thicknesses. Choosing just one height for a design can offer attractive benefits as discussed in the body of the text. Note that the contribution to height that comes from the solder ball is nominally in the range of 50% thus if low-profile packaging is desired elimination of the solder ball will deliver significant benefit.](image1)

![Figure 2. Elimination of solder and the use of a standard component heights and lead pitches opens the doors to unique capabilities for building low-cost high-performance electronic products. The aluminum cost two dollars per pound which is less than FR4 but also a superior thermal conductor and much more dimensionally stable. Moreover components can be placed on both sides and the aluminum can serve as a ground for the electronic assembly. Also of value is that such assembly is possible using all current PCB industry manufacturing infrastructure.](image2)
Reduction of voids in solder joints—an alternative to vacuum soldering

Rolf Diehm, SEHO Systems GmbH, Kreuzwertheim, Germany; Mathias Nowottnick, University of Rostock, Rostock, Germany; Uwe Pape, Fraunhofer IZM, Berlin, Germany

Abstract

Voids in solder joints are representing one of the main problems especially for power electronics. A low and homogeneous thermal resistance of solder joints is demanded for a quick and uniform conduction of the heat loss from the power chip. The same applies for the electrical conductivity of solder joints. Enclosed voids can cause a displacement of electrical and thermal paths and a local concentration of power and heat. In addition, gas voids are anxious to form spheres in the solder gap, which could be a cause for tilting of chip components and a wedge-shaped solder gap. This is tightening the problem of patchy distribution of current or heat and is causing stress and cracks.

The amount of voids can be influenced by different measures, e. g. a good wettability of metallization, solder pastes with special adopted solvents and an adequate preheating profile. However, a special vacuum process step during soldering is demanded for absolutely void free solder joints. But this vacuum process is associated with some essential disadvantages. Besides of the technical expenses for vacuum pumps and additional locks, the vacuum process excludes the use of gas convection for heating and cooling. Apart from a special vapour phase–vacuum technology, most machines are using infrared radiation or heat conduction for soldering.

The same principles as used in vacuum soldering technology are applicable also for a higher pressure level. If the void in the solder joint is arising for an excess pressure, the normal atmosphere pressure could be sufficient for escaping of enclosed gas. Essential for this effect is the pressure difference between inside and outside of solder joint. A benefit of soldering with excess pressure is the possibility of gas convection for heat transfer. This allows the application of conventional components and the realization of the usual temperature distribution and profiles.

Introduction

By the progress of failure detection in solder joints by X-ray analysis or X-ray computer tomography, the issue of voids in solder joints is currently discussed very intensively. The increasing demands on homogeneity of joints for miniaturization and applications of high temperature electronics also made a contribution to this discussion. The specifications about the acceptable amount of voids in solder joints were further concretized in IPC-A-610D. The maximum amount of voids for plastic BGA solder joints as well as for thermal plane terminations (D-Pak) is less than 25% in an x-ray image area. Design induced voids, e. g. microvia in land, are excluded from this criteria and will need to be established between the manufacturer and user. Just for special technologies, like chip-on-board for power applications, a smaller threshold can be established. For the conduction of high electrical or thermal currents not only the electrical and thermal conductivity of the connection, but also the homogeneity of the solder joints are very important. Especially voids and enclosures can impair this homogeneity. The result can be “hot spots” on the chip, which limits the useable power or could damage the components.

However, voids often have another negative influence on large-area solder joints. Because of the ambition of gas bubbles and liquid enclosures to minimize their surface, they will contract in the solder gap depending on the size. In the ideal case small voids can contract in the gap as spheres. Larger voids can lift the components or the chips on discrete positions, because of the limited dimension of gap. Since the distribution of voids in the solder gap is rarely uniform or few small voids can cumulate to larger voids, a tilting of component is the result as a rule. A high tilt intensifies inevitably the inhomogeneity, the non-uniform distribution of currents and temperature and particularly the thermo-mechanical stress. The thickness of solder gap, especially in connection with very different materials, such as silicone and copper for FR4, is very important for the adaption of the unequal expansions to temperature changing. The deformation of solder joints will be increased with the length of components edges, the difference of temperatures and the difference of thermal expansion coefficients and can be decreased with the thickness of solder gap. Since the materials and joining areas are given by the component and substrate types, the thickness or height of solder gap is usually the only chance for soldering technology, to reduce the deformation and the affiliated stress for the unavoidable temperature cycles. An unregulated tilt of components or chips can lead to a local concentration of stress and therefore to additional weak spots of the solder joint, which will reduce the life time or reliability.

Indeed, voids in solder joints are nearly inevitable for common process conditions. The ingredients of the solder pastes, which are evaporating during the soldering process, cannot exhaust completely especially for plane solder joints and closed gaps and will be enclosed in the solder joints. With the introduction of lead-free solders with the well-known difficulties of poor wetting and smaller process windows the problem has become more acute. Therefore the acceptable or established maximum void content can exceed frequently. Improved materials and processes should produce relief for that.

Process Influences

Various studies and investigations were devoted to the finding of optimum process parameters for prevention of voids. So it is possible that solder joints made of the same materials and with the same components but manufactured with different soldering profiles can show outwardly perfect behaviours but nevertheless they will have a very different void content inside. Especially because of the use of lead-free solders with a higher melting point, it could be neces-
sary to compensate the limited maximum of soldering temperature with an extension of soldering time (figure 1).

Figure 1 – Extended soldering time for compensation of a limited soldering temperature for higher melting lead-free solders

Even if the demanded adaptation of soldering profiles is able to transfer the same heat quantity and it is possible to realize the same visible result of wetting, the extended soldering process with lower temperatures will influence even so the speed and dynamics of soldering process. Because of the slower flow of solder and the higher viscosity of the melt for lower temperatures, flux residues can exhaust more poorly and form voids.

The Fraunhofer Institutes IZM and ISIT have investigated the forming and development of voids with more than 200 test boards in a joint research project [1]. Solder joints were observed by X-ray analysis also during the soldering process in this project. It was clearly visible that voids that have already been formed will never escape if keeping the soldering temperature. On the contrary, the apparent effect can be observed: the voids will be increased during holding of soldering temperature. But this is usually caused by the accumulation of several smaller voids, which are under the resolution limit themselves, into larger voids with clearly visible sizes. But there are also some cases, when voids can be formed by dewetting effects of component terminations or outgassing from PCB material during dwelling of soldering temperature.

Thus, a good and fast wetting is helpful for minimizing the amount of voids. A fast wetting which is able to transport the developing gases and residues out of the solder joints needs a certain minimum soldering temperature. This was shown clearly by systematic investigations with the wetting balance analysis. The interpretation of numerous wetting curves with different solder alloys and test temperatures results in a relation, shown in figure 2.

The desired fast soldering process requires a minimum soldering temperature of 10% above melting point (based on Kelvin scale), independent from the solder alloy. That means that a preferred soldering temperature for SnPb alloy is 229°C, but for SnAgCu the soldering temperature is already 266°C. Such high temperatures are usually prohibited for assembly processes because of sensitive components and printed circuit board materials. Thus, problems with an increased amount of voids in solder joints are expected.

Since the design of temperature profile and maximum soldering temperature is normally very restricted and the enclosed voids cannot be eliminated in a common soldering process, further improvements can be realized with appropriate preparation and treatment processes. With a pre-drying of the printed and assembled boards it should be possible in principle to reduce the amount of humidity of materials and volatile ingredients of solder pastes. Investigations have shown that for the optimized lead-containing solder pastes a pre-drying will effect rather a slight increase of void amount. However, figure 3 shows the evaluation of tests and, depending on manufacturer or flux type, also a considerable improvement of void content for SnAgCu solder pastes. At best it should be possible to achieve nearly the same low void amount as for SnPbAg solder pastes. One hour drying of assemblies above 100°C also eliminates absorbed water, in contrast to storage at room temperature.

Material Influences

Beside of the process, the applied materials also have an influence on the amount of voids in solder joints. As already stated above, a fast solder wetting gives a positive contribution to a reduced void content because of the higher dynamic. Therefore, solder alloys, fluxes, and surface metallizations are preferred which abet a fast and good wetting. Figure 5 shows the comparison of the results from investigation of voids on different printed circuit board finishes, NiP/Au (ENIG), immersion tin and copper/OSP.

While SnPbAg solder shows a similar low void content on all three surface finishes, clear differences for both tested SnAgCu solder pastes were detected. The lowest void content will be obtained on NiP/Au surface finish, which is able – in conjunction with pastes showing good wetting
behaviour – to realize similar good results like SnPbAg pastes.

Especially for reflow soldering of pre-soldered components such as BGA or CSP it is possible to minimize the amount of voids with a suitable combination of solder alloys [2].

If the solder paste is melting sooner than the alloy of the solder balls, the evaporating flux has a chance to escape from solder gap before the balls are melting. Because of that less gases and residues will be enclosed in the solder joints. These statements can be confirmed by experimental work. Figure 6 shows the result of these trials in an X-ray image.

**Special Processes**

All measures of process and material adaptation discussed so far can only give a contribution to minimize the number and size of voids. In this way a general elimination of voids is hardly possible.

The most effective measure against voids is the application of a vacuum process during soldering, which is able to suck off gases and flux residues from the joint, as long as the solder is molten. The effect is clearly visible when looking at the soldering results in X-ray images, shown in figure 7. By means of a vacuum process it is possible to eliminate the voids and enclosures almost completely.

The special demands of power electronics may sometimes legitimate the extraordinary efforts of a vacuum process. It is, however, advisable to select the solder materials especially for this vacuum process, since some flux ingredients incline to extreme foaming and blistering so that components can be replaced or uplift potentially. Apart from the choice of solder paste, the process can be adapted in such a way that the vacuum will not affect until the predominating part of the solvents is evaporated.

However, there are several disadvantages of a vacuum process. Printed circuit board materials and also some components are tending to excessive outgassing in vacuum. Therefore, the targeted vacuum pressure will be achieved very slowly. Also some electrolyte capacitors cannot tolerate the vacuum process because of the hermetically enclosed liquids. Another drawback is that heat cannot be transferred in the vacuum with the usual convection heating but only by means of infrared radiation or heat conduction. Both heating methods are not sufficient for the use on printed circuit boards. Some of the present soldering machines are using the fast and effective heating with vapour phase with a subsequent vacuum process [3]. The assemblies have to be heated sufficiently during this soldering process, so that the solder is still liquid in the following vacuum process. To ensure a minimum thermal exposure it is essential to achieve a fast transition from the soldering zone into the vacuum area which requires a powerful lock and pump system as well as optimum vacuum pressure.

Various experimental series were conducted to find the necessary pressure for the intended vacuum soldering process. A significant reduction of voids in solder joints was observed below 700 mbar. Obviously, voids in BGA and CSP solder joints are very intractable. Particularly removal of design related voids it is very difficult or even impossible. An example of a typical void in a BGA solder joint is shown in figure 8 which displays the geometrical relations.

Following the Young-Laplace equation it is possible to calculate the pressure relations of such a void: \( \Delta p > 2 \sigma / r \)

Apart from the measured radiuses the surface tension of the liquid solder (\( \sigma \)) is also important for the calculation. Own measurements of liquid solders (pending drop method) have resulted in a surface tension of 448 mN/m for SnPb and 548 mN/m for SnAgCu. Another reason for the higher amount of voids in lead-free solder joints or the difficulties to remove them is this significantly higher surface tension. With the data from the example above it is possible to calculate that a minimum of 100 mbar pressure difference between inside of void and its environment is necessary to remove this void. This means, that after soldering at normal pressure, the ambient pressure must decrease to 900 mbar or less in order to remove this void.

New considerations were proceeding on assumption that for the removal of voids it is not the absolute vacuum pressure that is important, but much more the difference of pressure between void and environment. This consideration leads to the inference that it should also be possible to remove a void at normal pressure if it was formed at excess pressure [4]. The advantage of this conception is obvious because a soldering process with overpressure allows heating of assemblies with forced gas convection, with similar thermal behaviour like standard reflow soldering and all its advantages, such as low temperature differences (delta T), good heat transfer and controlled heating process. Moreover, outgassing materials and leaking components are not likely to result from a soldering process with elevated pressure.

Due to the fact that the currently available soldering machines are technically not prepared to work with overpressure, a simple laboratory setup was improvised for the first principle tests. An espresso pot which is designed for a pressure of 2 bar was rebuilt and used for these tests. The soldering samples were molten in this pot with overpressure and afterwards, in the liquid state of the solder joint, the atmosphere was released to normal pressure by opening an outlet. After first successful tests with heat conduction on a hot plate with DBC substrates and soldered Si chips, further lab setups were developed. This solution consisted of a greater pressure container which included a controlled heating, even a forced convection fan could have been installed (figure 9).
A standard FR 4 printed circuit board with large-area solder joints was selected for the first tests (figure 10).

Using the pressure container from the laboratory setup it was possible to vary the pressure conditions while temperature and other process parameters were kept on the same level. Figure 11 gives a small insight in possible temperature profiles and resulting solder connections with associated voids.

Based on these findings a reflow soldering system with convection preheating area and pressure chamber in the peak area was developed and introduced during Productronica 2011. The preheat area of this system completely corresponds to a regular reflow soldering system. The modified peak area consists of a specially designed pressure module in combination with a convection heating zone (figure 12). Compared to vacuum soldering, this solution provides the advantages of usual reflow soldering technologies. That means it is possible to heat the assemblies homogeneously and effectively by forced convection in either an ambient or nitrogen atmosphere.

First test series with this oven confirmed the positive approach of the laboratory tests. Overall, a high pressure zone provides a higher efficiency and more flexibility than a vacuum process. Whereas the pressure level for vacuum processes ranges between 1 bar (atmospherical pressure) and 0 bar, a high pressure zone allows a process range between 4 to 5 bar and 1 bar. Most noticeable, however, is the dynamics of pressure. As discussed earlier, a certain vacuum which would be able to remove voids only can be reached slowly and in addition this requires expensive pump technique. Less mechanical construction is needed to reach a high pressure range of 4 – 5 bar which can be released instantaneously to make voids leave the liquid solder depot (figure 13).

The following pictures and graphs demonstrate the test boards and results which could be obtained.

Conclusions
The smaller process window for lead-free soldering does not allow much clearance for optimizing a void-free process. With best possible conditions including optimized fluxes and surfaces showing a good wetting behaviour, the amount of voids can be reduced.

A nearly void-free solder joint, often demanded for assembling of power electronics components, definitely only can be realized by variation of the atmospheric pressure. A variety of vacuum soldering processes were established in the past which use infrared radiation, heat conduction or the combination with vapour phase soldering for heating.

The same principle of pressure difference is used for soldering with elevated pressure and a sudden pressure release to normal level (hyper pneumatic soldering). This new technology allows forced convection for heat transfer during the reflow process with all its well-known advantages.

References
The hoped for the “2012 recovery” has met with a number of recent roadblocks as evidenced by the May decline in the JPMorgan Global Purchasing Managers’ Index (Chart 1).

Growth obstacles include:
- Europe’s major economic woes, resulting declining industrial output (Chart 2) and the struggles to keep the EU and its common currency in tact in the face high debt and minimal liquidity in Greece, Spain and Italy.
- Japan’s very strong yen (Chart 3) limiting its exports.
- U.S. political wrangling bringing legislative progress to a standstill.
- China, Taiwan and S. Korea’s dwindling export prospects as it its normal customers struggle with weak economies.

As measured by global electronic equipment production (Chart 4), May should have been the bottom of the normal seasonal trough with significant growth resuming in June and then extending through the pre-Christmas “busy season.” Unfortunately based upon today’s weak global markets the 2012 summer/fall growth seasonal spurt will probably be throttled by low consumer and industrial demand.

Despite the current economic headwinds there are signs of a seasonal pickup. One optimistic indicator is Taiwan wafer foundry sales (Chart 5), which historically have been a leading indicator for global semiconductor shipments (and hence world electronic assembly activity). Hopefully the May wafer foundry sales spurt portends an imminent seasonal upturn in 2012! We hope so but we are not sure.

Charts 6 and 7 summarize our colleague Ed Henderson’s most recent forecasts for world GDP and electronic equipment production by region. For more details see www.hendersonventures.com.

End Markets
China’s IT equipment consumption is expected to increase to US$173 billion in 2013, 4 percent more than that of Japan. —IDC

Computers & Peripherals
- Total PC shipments are expected to rise 15 percent y/y to 478 million units in 2012. —IC Insights
- Mobile PC shipments fell 15 percent y/y to 76.2 million units in 1Q’12 but grew 30 percent y/y; tablet PCs grew 124 percent y/y and notebooks and mini-notebooks grew 12 percent. —NPD DisplaySearch
- Tablet shipments reached 18.2 million devices in 1Q’12; Apple accounted for 65 percent or 11.8 million of the total shipments. —ABI Research
- Workstations shipments reached 918.4 thousand units in 1Q’12. —Jon Peddie Research
- Worldwide server shipments grew 1.5 percent in 1Q’12 to 2.3 million units while revenue declined 1.8 percent to $12.4 billion. —Gartner
- Global server revenues fell 2.4 percent to $11.8 billion in 1Q’12. —IDC
- Global enterprise router market declined 9 percent to $834 million in 1Q’12. —Infonetics Research
- Global service provider router and switch market decreased 14 percent to $3.3 billion in 1Q’12. —Infonetics Research
- Global wireless LAN equipment revenue fell 4 percent q/q to $859 million in 1Q’12. —Infonetics
- VoIP equipment market increased 1 percent q/q to $715 million in 1Q’12. —Infonetics Research
- Worldwide external disk storage sys-
tems factory revenues increased 7.1 percent y/y to $5.99 billion in 1Q’12. — IDC
• Graphics add-in board shipments fell 2 percent q/q to 15.8 million units in Q’12. — Jon Peddie Research

Mobile Communications
• Worldwide mobile phone shipments are expected to grow 4 percent to 1.8 billion units in 2012. — IDC
• Worldwide mobile phones sales (budget, midrange, feature and smartphones) to end users declined 9 percent to 379 million units in Q’12. — Forward Concepts
• Connected car solutions will grow from 66 million units in 2012 to 356 million in 2017. — ABI Research
• China mobile subscribers rose 1.1 percent to 1.02 billion users in April 2012.

EMS, ODM & Related Assembly Activity
3CEMS’ South China facility, Broad Technology received IECQ QC080000 certification for Hazardous Substance Process Management.
API Technologies’ EMS Business Unit reduced head count by 40 positions.
Artaflex
• acquired Adeptron.
• named Frank Sherl CF0. CB Technology installed a MYDATA MY100LX14 pick-and-place machine.
Computrol installed an additional KISS 103 selective solder system from ACE Production in Meridian, Idaho.
EMS-Electra purchased an in-circuit test system from Dr. Eschke Elektronik GmbH.
Enics received AA-level customs certification in China.
Fascia Graphics invested in pick & place technology.
Foxconn/ Hon Hai Precision
• invested USD210 million for new Apple production line in Jiangsu, China.

Japanese Yen vs. U.S. Dollar

World Electronic Equipment Monthly Shipments

Technical Manufacturing received ISO 9001:2008 and AS 9100C certifications.
Variosystems broke ground on its 120,000 SF facility in Suzhou, China.
Videocon set up a manufacturing unit in Kerala, India.
Invotec was sold to RG industries.
Marl International added a DEK Horizon 03IX print platform.
National Physical Laboratory, In2Tec and Gwent Electronic Materials developed PCBs with components that can be easily separated by immersion in hot water.
P. D. Circuits received ISO 9001:2008 recertification.
Schweizer Electronic introduced HDI and RF combi boards.
TC ORI LIGHT sold 51 percent of share capital in PCB subsidiary ISU TC CO.
Viasystems completed its DDi acquisition.
Westak celebrated 40 years of PCB manufacturing.
Zhen Ding will invest THB530 million (US$16.7 million) to add buildings at its PCB factory in Thailand and an additional THB500 million in production equipment.

**Materials & Process Equipment**

Advanced electronic materials are projected to increase at a 5-year, 36.3 percent CAGR from $27.6 million in 2010 and $30.7 million in 2011 to more than $5.5 billion in 2016 and almost $26 billion in 2021.

China’s general purpose test equipment market is forecast to grow at a 5-year 9.4 percent CAGR from $415.9 million in revenue in 2011 to $713.5 million by 2017.

Frost & Sullivan

Conductive ink market will grow from $2.86 billion market in 2012 to $3.36 billion in 2018, with $735 million captured by new silver and copper nanostructure inks.

Frost & Sullivan

Agilent bought Dako for $2.2 billion.

AimCore expanded its ITO coating capacity to 10 lines.

Airtech achieved ISO 9001:2008/AS9100 Rev C.

Arlon Material Technologies doubled its lamination capacity in Suzhou China.

Asahi Kasei is constructing a PCB dry film photoresist manufacturing plant in China with an annual capacity of 120 million sq. meters.

Csun opened a TFT LCD, PCB and semiconductor equipment plant in Taichung, Taiwan.

Datset installed a XD7600NT500 Ruby X-ray inspection system with X-Plane™ technology from Nordson DAGE.

Data I/O appointed Brian Crowley to its Board of Directors.

Dow Chemical promoted Bhavesh Muni to Global Business Director of Advanced Packaging Technologies.

Elite Material is building a CCL fabrication plant in western China.

Hitachi High-Technologies purchased Seiko Instruments’ subsidiary that specializes in analytic, measurement and observation instruments.

Indium

- named Robert Ploessl Ph.D. as product manager for indium, gallium, germanium and tin compounds.

Isola celebrated its centennial anniversary.

Juki Automation Systems celebrated the shipment of 25,000th machine.

Kaneka Malaysia began construction of a polyimide film plant.

Koh Young delivered its 3000th 3D in-line SPI system to Mack Technologies.

Maskless Lithography named Mark Wolfenbarger North American Sales Manager.

Nordson MARCH appointed Carla Loeffler Western Regional Sales Manager.

Semiconductors & Other Components
Worldwide semiconductor shipments will rise 0.4 percent in 2012 to $300.8 billion.

GDP Growth

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Electronic Equipment Production Growth

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The most highly regarded global assembly journal for SMT and advanced packaging professionals, Global SMT & Packaging features solution-led technical articles, case studies, insightful columns, event reports and much more. The print magazine comes out in four editions: Europe, Americas, China, and South East Asia. We also have websites and newsletters for Mexico and Brazil. Start at www.globalsmt.net
MYDATA has had a very successful 2011/12 so far. Can you tell us what has been driving that performance?

Certainly, I am happy to be asked this question after such a successful year as 2011. We grew by 31%, which follows on from 2010 when we also grew by 30%, so we have emerged strongly from the downturn in 2009 and left it far behind us.

The reasons for our success are many fold. In part it is because of changing general market trends, which particularly suit our machines. Customers need more solutions to cope with ever increasing complex-
ity in the production environment. High mix is increasing and his is what MYDATA is all about. We don’t only think about our pick ‘n place machine and what is happening inside the pick ‘n place machine, but we think about the whole concept about delivering the highest possible performance in a complex manufacturing environment. Taking into account the machine itself where we not only have intelligent feeders, but the machine itself is intelligent and we have a very large system code that is optimizing itself constantly. Beyond that we have a software suite that ties it all together. We have a production planning system, a logistics systems coupled to our intelligent source system. Everything that helps our customers navigate in a high-mix, complex environment, which is very disruptive in nature.

In addition to that we not only service a large existing customer base, but we have a high number of new customers coming to us every year and we are seeing 30-35% of our pick ‘n place sales to new customers.

How much has the market shift towards mid-volume manufacturing helped you?
The market trend is coming our way which is one big important. The other important component is that our product portfolio is very strong. Last year we introduced the e-series machines, which delivers a speed increase of over 20% from it’s predecessor. We have introduced today the higher end model, the MY100HXe which has a throughput of 50,000cph.

Can you tell us what are the strengths of your MY500 printing platform?
With the MY500 jet printing system you can optimize the individual volume of paste per pad, which enable you to produce high quality, high yield boards with the machine and you don’t need stencils. It’s a software driven system that is ideal for all applications from prototyping to medium-volume production. It is extremely flexible and suits the high-mix environment.

How much of your sales growth can be attributed to the jet printers?
We grew the jet printing business by more than 57% last year, which was a significant increase. According to PROTEC we captured 15% of the overall printer market in Europe.

Let’s go back to the pick ‘n place platform for a moment and the development path for your e-series. Your fellow European competitors such as ASM and Assembleon are pursuing the sub 10µm market for highly accurate placement, whereas the Japanese manufacturers are building more functionality into the machine. Which strategy is MYDATA following?
There is no question that we will stay on the current development path to deliver the best possible functionality for the high-mix environment. We will expand that scope over time to address that growing market segment. With that we will continue to develop the machines, better price performance as a basis, but also developing the functionality around it, developing our software suite, feeded loading and so on.

Robert, thank you for joining us today.

Editor’s Note: You can view the full interview on video by clicking on the embedded video on this page, or by visiting Global SMT TV on the website at www.globalsmt.net
Why perform failure analysis?

Craig Hillman, PhD

Why do you perform failure analysis? This question is often phrased as a business decision. Using Harvard-approved algorithms, weigh the cost of failure analysis (time, materials, resources, personnel, outsourcing, etc.) versus the benefit (corrective action, continuous improvement, retain market share, etc.) and determine if you have a sufficient return on investment.

But, what if the question was directed to the person performing the failure analysis? That is, why did you pick this career in the first place? I will admit that, after having performed failure analysis for almost fifteen years, I can sometimes feel like the pejorative mother-in-law in the back seat. The design team has the good fortune / blessing to be involved in the creative / creation process while the failure analysis / reliability team can end up being the “nattering nabobs of negativism” (if you get that joke, congratulations. You are pre-Internet).

But, there is nothing like a good detective story, and failure analysis can be that in spades. The best failure analyses I have been involved in required a methodical process, a splash of ingenuity, and drew upon a wide range of disciplines to solve the mystery. The brief example below will hopefully give you a sense of that adventure and excitement that is at the core of a good F/A.

Some time ago, my company, DfR Solutions, was approached by a large electronic retailer (not your typical F/A client, so you know this is going to be interesting). They were having an issue with game controllers. Hundreds of customers were receiving payment for turning in used game controllers. Problem was the controllers stopped working soon after the retailer had no idea why (cue Superman theme song).

The first step, in one of the longest F/A investigations we have ever been a part of, was to figure out what part in the game controller was failing. Based on the age of the controllers and the intermittent behavior (most likely failing at the customer, working when turned in, failing again soon after), the most likely failure mechanism was an interconnect somewhere in the system that was degrading over time.

So, as in most F/A investigations of electronics, our Electrical and Computer Engineering team used combination of electrical probing, trouble shooting, and investigation of fault codes to narrow down the failure site to the Graphical Processor Unit (GPU). Once the failure site is located through electrical engineering and software activity, a good F/A process requires that this initial identification be validated.

How to validate a failed part? The classic way is remove and replace with a known good device. When a separated interconnect (solder joint, wire bond, etc) is suspected, the failure site confirmation process can be simplified by trying to massage the interconnect through temperature changes (cold spray) or mechanical changes (pressing on the component). However, confirming the failure site was the easy part. Knowing which interconnect was the issue and why it failed was the real challenge.

Once failure site confirmed, the next step is to perform non-destructive evaluation (NDE). The GPU had two flip chip die (GPU and memory chip) on a ball grid array (BGA) substrate. Standard non-destructive techniques, such as high resolution (sub-micron) three dimensional X-ray and acoustic microscopy, were unable to show any evidence of degraded or cracked features at any of the interconnect levels (solder bump, solder ball, plated through hole). So what next?

In this situation, the right step is dependent upon the number of samples available. If there was only one failed unit, an appropriate NDE would be time domain reflectometry (TDR). TDR sends high frequency electrical signals into electrical nets and captures transitions and potential opens by the timing and shape of return pulses. While it is a really neat tool, TDR can be expensive, difficult, and the results are not always definitive or intuitive. In this case, since there were so many failures, a quicker approach with some trial and error and intuitive thinking can be used. Trial and Error: Dye and Pry, which involves flooding the BGA with dye and the prying it off the board, determined the BGA solder joints were intact. Intuitive Thinking: Since the GPU die is larger and hotter than the memory die, it is the more likely site of the failed interconnect.

Cross-sectioning of the flip chip GPU die quickly confirmed the presence of cracked solder bumps. For most F/A labs, this would be the end of the story. This failure analysis, however, required another level of ‘Why’ because the customer wanted to fix the game controllers without replacing the GPU. And you can’t fix something unless you know why it failed.

The key clues to root-cause were seen in the cross-section and they came from the Mechanical Engineering team. They noted an elongation of the solder bump, with bumps on failed units having a stretched oval shape. This elongation suggested that the solder bump was seeing out of plane tensile stresses, rather than the classic distance-to-neutral point (DNP) shear stresses that are often a concern with this configuration. The cracked bumps were also not located near the corners, typically associated with DNP behavior, but were more randomly distributed.

However, why solder bumps would see tensile stress (how many Whys have we answered at this point?) could not be answered until the Materials team performed analysis of the underfill. They quickly noted the glass transition temperature (Tg) of the polymer-based under-
fill was relatively low (around 65°C). If the GPU operation was near or above this temperature, the underfill would undergo dramatic changes in material properties. Working together with the Mechanical team, they realized that the sequence of material changes, with the coefficient of thermal expansion (CTE) increasing rapidly before a subsequent drop in elastic modulus, would place the solder bumps under an enormous amount of tensile stress. With tensile stress being far more damaging to solder than shear stress (not enough space in this column to explain), this condition was sufficient to explain the root-cause of failure. Simulation and modeling of the specific architecture and environments demonstrated results in line with observations of time to failure in the field.

However, the best part of this F/A was not just the numerous fields (electrical, mechanical, materials, thermal) required to identify the root-cause. It was being able to use this knowledge to solve the problem. With simulation and modeling demonstrating that the effect was very sensitive to temperature, DfR was able to recommend a change in the bios to cool the GPU sufficiently to prevent future failures.

Realizing the failure site was the solder bumps allowed us to create a specialized block heater that placed the flip chip under enough pressure and temperature to reflow the bumps and cure the fault.

And why is solving the problem the best part of failure analysis? Because, if you do your job right, you have just made somebody’s life easier. And isn’t that a nice thing to do?
Count On Tools Rolls Out PB Swiss Tools’ Rainbow SwissGrip Screwdrivers

Count On Tools Inc., a leading provider of precision components and SMT spare parts, announces that it now carries PB Swiss Tools Rainbow SwissGrip Screwdrivers. The new Rainbow Series color-coding makes it easy to quickly locate, assign and safely apply the right SwissGrip Screwdriver.

A combination of colors, performance and comfort — the trend towards colors continues. Three new screwdriver sets for Slotted, Phillips and Torx® screws with color-coding in a wall bracket are available in the new expanded assortment. The soft handle coating made of skin-friendly Santoprene® transfers high torque effortlessly. Each Rainbow Series tool is labeled with the serial number for additional security, and to enable tracing the production back to the raw material.

The color-coded features of PB Swiss Tools’ Rainbow Series set them apart from the rest by giving an indication of size to every tool. PB Swiss Tools uses the latest high-tech processes to manufacture colored handles and blades to make work better, easier, and more efficient.

The Rainbow SwissGrip Screwdrivers are available as individual tools or in a set featuring a convenient plastic wall rack. With more than 130 years of experience PB Swiss Tools is a global leader of hand tools manufactured for use in the industrial marketplace, even for the most hazardous jobs. All PB Swiss Tools are 100 percent Swiss-made and come with an unlimited lifetime guarantee. Work with the best. www.pbtools.us.

LPKF Integrates Advanced Capabilities in the New MicroLine 6000 P

LPKF introduces the next generation of the MicroLine 6000 P, a UV laser system designed for etching, drilling, cutting and depaneling of PCBs. New capabilities focus on precision and low-cost, making it a valuable asset for any fabrication process.

LPKF Laser & Electronics, a leading manufacturer of laser and electronics systems, presents the new MicroLine 6000 P, a flexible and reliable solution for processing printed circuit boards. By eliminating mechanical stress to boards and components, as well as debris and extra tooling costs, the UV laser system allows for more designs to be created in a short amount of time. The MicroLine 6000 P represents the next generation in LPKF lasers by increasing production planning and lowering total cost of ownership.

Focusing on precision, speed and accuracy, new capabilities of the MicroLine 6000 P include automatic beam correction for environmental interference, and an advanced vision system for more reliable, higher yield. The new system also delivers operative parameters, machine data, and tracking and tracing values as well as information about individual production runs. With a working area of 21×24” and reduced maintenance requirements, the new MicroLine 6000 P masters the balance between high quality, throughput and low cost.

SolderLab.com Debuts PotWatch Service

SolderLab.com, an independent solder analysis lab, introduces an innovative new service called PotWatch. Featuring easy-to-use Web-based ordering, PotWatch provides the user with a scheduled method for testing, tracking and validating their solder pot alloy purity.

With PotWatch, solders within most
tin/lead and SAC alloy matrixes are tested to J-STD-006B standard. Solder collection kits are mailed automatically to SolderLab.com customers at the timing and frequency of their choice.

SolderLab.com’s PotWatch process takes full coverage monitoring and testing of your solder pot to the next level, and makes the chore of solder purity and compliance testing simpler and safer than ever. Once signed up for PotWatch, SolderLab.com takes over the responsibility of maintaining its customers schedule for solder testing.

**DISCOVER PotWatch:**
To begin service, visit www.SolderLab.com, log in, and place an order. Your order will specify how often testing is needed and how many samples are required for each test interval. At the appropriate times, SolderLab.com will send an e-mail notification to advise you of your next test date, and will follow up with the delivery of the PotWatch Solder Collection Kit. With the solder collection cup included in the kit, simply fill it with solder, fill out the enclosed sample information card, attach the prepared return address label on the same envelope and mail it back. Within a few days of receiving your sample, you will receive a detailed SolderLab.com Certificate of Analysis via e-mail. The service is available at various intervals, and samples can be scheduled on a monthly, quarterly, bi-annual or annual basis. www.SolderLab.com.

**Engineered Conductive Materials Debuts 530-121 Low-Cost Conductive Adhesive**
Engineered Conductive Materials, a leading global supplier of conductive interconnect materials for photovoltaic applications, introduces the new 530-121 low-cost conductive adhesive designed for ribbon stringing in tin-based solar modules. The price of this material formulation is 60 percent of the cost of a pure silver-filled material and has been optimized for excellent conductivity and stability on various substrates when cured at 150°C.

The 530-121 has a dispensing work life greater than 48 hours (measured as a 25 percent increase in viscosity), while maintaining optimized rheology for dispensing and excellent damp heat resistance. Also, the material has conductivity stability on molybdenum and tin, tin-silver and silver-plated ribbons. The 530-121 features a rubber-like flexibility that is ideal for flexible photovoltaic applications with high peel strength to withstand the stresses induced in reel-to-reel manufacturing processes. This material also can be fast cured at elevated temperatures (2 minutes @ 180°C).

530-121 is the latest addition to Engineered Conductive Materials’ full line of conductive stringer attach adhesives, conductive adhesives for back contact crystalline silicon, thin-film and via fill applications, as well as conductive grid inks for photovoltaic applications.

For more information about the 530-121 Conductive Adhesive or to learn how Engineered Conductive Materials can define, develop and create an engineered material solution that is right for your company, visit www.conductives.com.

**Techcon Systems Adds 32-Pitch Feed Screw to TS7000 Series for Microdot Dispensing**
Techcon Systems, a product group of OK International and a leading provider of fluid dispensing systems and products, today announced the addition of 32-pitch TS7000 model to the TS7000 Valve Series.

The TS7000 Series now is available in four sizes: 32-pitch, 16-pitch, 8-pitch standard and 8-pitch high output. The new, finer 32-pitch feed screw is designed to dispense microdot sizes (as small as 0.010” or 0.25 mm diameter) with a high degree of accuracy and repeatability.

“ ” commented Can La, Product Manager of Techcon’s Industrial Products Division.

The TS7000 IMP Series Valve provides fast, repeatable dispensing of medium- to high-viscosity fluids and pastes. Typical applications include small-dot dispensing of dispense-grade solder pastes, silver epoxies, surface mount adhesives, dispensing beads of structural adhesives, cavity & cam filling, and glob top dispensing.

For more information about Techcon System’s TS7000 Interchangeable Material Path Series Rotary Valve, visit www.techconsystems.com.
IPC APEX EXPO Named In Top 25 Fastest-Growing Trade Shows
Sold Out Show Floor Predicted for 2013
IPC – Association Connecting Electronics Industries* announces that IPC APEX EXPO® has been named one of the Trade Show News Network 2012 “Top 25 Fastest-growing Trade Shows in Attendance in the United States.”

IPC Vice President of Industry Programs Tony Hilvers says that the show met or surpassed all attendance and exhibition goals in 2012 and is now 90 percent sold out for 2013 with 11 percent more square footage sold than at the same time in 2012. He adds, “We are at 113,000 sq. ft (10,500 sq. meters) and we expect to sell out.”

IPC APEX EXPO was founded in 1994 to provide a cost-effective exhibition focused on the printed board industry. The event later expanded to include the electronics manufacturing industry as well. Hilvers explains, “This show was created by our members to meet the need to bring customers and suppliers together in an educational and mutually beneficial arena. Every decision that’s been made through the years has been made to improve the event for the participants.”

Over the years, industry members have found IPC APEX EXPO to be an excellent venue for networking, education and finding and comparing suppliers. “Being able to discuss technical details with various suppliers opened my eyes to how willing and able suppliers are to help solve my problems,” notes Joshua Garrett, process engineer, Minco Products Inc.

IPC APEX EXPO 2013 conference and exhibition will take place February 19-21, 2013, at the San Diego Convention Center. Companies interested in exhibiting should visit www.IPCAPEXEXPO.org or contact Mary Mac Kinnon, IPC director of trade show sales, at +1 847-597-2886 or MaryMacKinnon@ipc.org. More information on the Trade Show News Network is available at www.TSNN.com.

IPC Puts It to a Vote: Asks Who Will Be 2013 IPC APEX EXPO Keynoter? Deep Sea Explorer, Physicist, Movie Producer or Astrophysicist?

Just as IPC standards are balloted by industry, the decision of who will be the 2013 IPC APEX EXPO Opening Keynote speaker is in the hands of the electronics manufacturing industry. IPC is asking industry to decide who would be the ideal keynote speaker to kick off three days of inspiring information and knowledge at IPC APEX EXPO 2013, February 19–21, in San Diego.

An impressive ballot, the four candidates are: Dr. Neil deGrasse Tyson, an astrophysicist; Jon Landau, Academy Award®-winning producer; Dr. Michio Kaku, a physicist and author; and Dr. Robert Ballard, deep-sea explorer.

Each speaker has stories and experiences that captivate and entertain their audiences, but IPC is hopeful that the voting will determine who can do more than that for the show’s attendees. “IPC APEX EXPO is not just a conference and exhibition,” says IPC President & CEO John W. Mitchell. “It’s an ‘experience.’ Each year committee volunteers and staff work together to design the ideal learning environment that not only encompasses leading experts, top suppliers and breaking and innovative research, but also sets the stage for three days of creative problem solving and ‘Aha’ moments.”

Dr. Tyson’s professional research interests include star formation, exploding stars, dwarf galaxies and the structure of the Milky Way. During the Bush administration, he served on a nine-member commission on the Implementation of the United States Space Exploration Policy and in 2006, he was appointed to serve on NASA’s prestigious Advisory Council. Dr. Tyson also hosted seasons two through five of NOVA scienceNOW.

Jon Landau produced the two highest grossing movies of all-time, Avatar and Titanic. In his engaging presentations, Landau not only shares insight into the film industry and the complex state-of-the-art visual effects technologies, but also discusses the broader perspective of business management, innovative marketing and motivational philosophies, encouraging audiences to be leaders — not just in their careers, but in their lives as well.

Dr. Michio Kaku is an internationally recognized authority on Einstein’s unified field theory which he is attempting to complete, and predicting trends affecting business, commerce, and finance based on the latest research in science. He is the author of several international bestsellers, including Physics of the Future: How Science Will Change Daily Life by 2100.

Among the most accomplished of the world’s deep-sea explorers, Dr. Robert Ballard is best known for his historic discovery of the RMS Titanic 12,000 feet/4,000 meters under the North Atlantic. Using the latest in exploration technology, he has conducted more than 100 deep-sea expeditions leading to many lost legend discoveries, including the German battleship Bismarck, the aircraft carrier USS Yorktown, and U.S. President Kennedy’s PT-109.

To learn more about the four keynote candidates and to vote, visit www.IPCAPEXEXPO.org/keynote-vote. Voting will be open until June 22, 2012. The winner of the IPC’s keynote contest will be announced in late August.

Executives to Experience Electronics in the Fast Lane at IPC Midwest

“Electronics in the Fast Lane: How High Speed Technologies are Changing the Game,” will be the theme of the IPC Executive Summit, August 21–22, 2012, in Schaumburg, Ill. This year’s event will be held in conjunction with the IPC Midwest Conference and Exhibition®, giving attendees the opportunity to see the latest in equipment, processes and materials.

The event will begin with the keynote presentation, “Electronics Industry and Economic Trends,” by Randy Bane, vice president and chief economist, Applied Materials.

The morning program will also include
a presentation by Mike Freda, interconnect specialist, Oracle America, Inc., “How to Achieve High Speeds without Breaking the Bank,” as well as a panel discussion on new materials featuring experts from Isola Group SARL, Rogers Corp., Park ElectroChemical Corp., and Ventec USA.

Breakout sessions in the afternoon will offer separate management meetings that focus on business issues specific to three segments of the industry. The EMS Management Meeting will explore lean sigma in electronics manufacturing, and creating and following an EMS dashboard. In the PCB Management Meeting, presentations will address standards impacting the industry, meeting customer needs, and how to break into the HDI and embedded markets. The PCB Supplier Management Meeting will cover best practices of innovation and bringing new products to market. All of the management meetings will conclude with roundtable discussions.

A half-day marketing workshop will be offered as an alternative to the management meetings. “B2B Marketing in a Digital Age” will be presented by two senior consultants and electronics industry specialists from Protean Marketing Communications, Rich Heimsch, director, and Greg Robinson, co-owner and director. The workshop will provide valuable techniques in branding, implementing digital marketing tools and measuring results, all geared toward the electronics manufacturing industry.

The second day of the IPC Executive Summit will begin with the IPC Midwest opening session, “Nanotechnology and Electronics Assembly,” by Alan Rae, Ph.D., CEO, NanoMaterials Innovation Center. Other featured technology presentations on the second day include “Best HDI Markets in North America,” by Michael Carano, director of global business development & strategic marketing, OMG Electronic Chemicals; and a session on the market potential for fiber optic applications.

The changing business environment will be discussed in three sessions on environmental policy, on-shoring and the electronics industry in Latin America.

www.IPCMidwestShow.org/Executive-Summit.

IPC/ JEDEC-9704A Takes the Stress Out of Strain Gage Testing
Joint Industry Guideline Provides Best Practices for Measuring the Strain on Boards and Components During Manufacturing
Put a fair amount of stress on the bond between printed boards and electronic components and there's a chance problems will arise, from solder ball cracking to conductor damage to pad cratering. Although measuring stress was a challenge for EMS and OEM companies, the recently updated joint industry guideline, IPC/JEDEC-9704A, Printed Circuit Assembly Strain Gage Test Guideline, makes it easier for engineers to run strain gage tests during the manufacturing process.

“Revision A is about making sure there's a common accepted practice for measuring manufacturing strain on printed board assemblies due to board flexure,” said Jagadeesh Radhakrishnan, a reliability engineer with Intel Corp. and leader of the effort within the IPC SMT Attachment Reliability Test Methods Task Group that helped revise the guideline. Whereas the first-generation document provided industry with target pass/fail points, the A revision, as Radhakrishnan explains, “…changes the focus to providing a methodology. It doesn't give you targets; it thoroughly explains how to measure strain.”

Revision A includes formulas for calculating strain and describes techniques for analyzing data derived from these tests. The tests can be performed at many stages during the manufacturing of printed board assemblies. Components can be tested during assembly or during test processes in the factory or just before they're packaged.

In addition to the change in focus, IPC/ JEDEC-9704A has an expanded scope and provides recommendations for sockets and ceramic capacitors; in the past, it just addressed ball grid arrays (BGAs). “It also changes parameters for in-circuit test fixtures, providing best design practices so users will have fewer issues,” adds Radhakrishnan.

IPC/JEDEC-9704A is available for purchase by IPC members for $36. The standard industry price is $72. For more information or to purchase IPC/JEDEC-9704A, visit www.ipc.org/9704.

IPC releases PCB industry results for May 2012
PCB Industry Growth Rates and Book-to-Bill Ratios Announced
Rigid PCB shipments were down 1.9 percent in May 2012 from May 2011, but bookings increased 12.0 percent over year. Year to date, rigid PCB shipments decreased 5.0 percent and bookings increased 3.1 percent. Compared to the previous month, rigid PCB shipments were up 2.0 percent and rigid bookings gained 1.9 percent. The book-to-bill ratio for the North American rigid PCB industry in May 2012 remained above parity at 1.02.
Flexible circuit shipments in May 2012 were down 10.0 percent, and bookings were down 1.1 percent compared to May 2011. Year to date, flexible circuit shipments decreased 9.1 percent and bookings decreased 2.1 percent. Compared to the previous month, flexible circuit shipments decreased 2.6 percent, but flex bookings were up 19.8 percent. The North American flexible circuit book-to-bill ratio remained high at 1.17.

For rigid PCBs and flexible circuits combined, industry shipments in May 2012 decreased 2.6 percent from May 2011 and orders booked increased 10.6 percent from May 2011. Year to date, combined industry shipments were down 5.3 percent and bookings were up 2.6 percent. Compared to the previous month, combined industry shipments for May 2012 increased 1.7 percent and bookings increased 3.3 percent. The combined (rigid and flex) industry book-to-bill ratio in May 2012 decreased slightly but continued in positive territory at 1.03.

“North American PCB sales and orders in May continued slightly below last year’s levels and reflected normal seasonal patterns,” said Sharon Stapp, IPC director of market research. “The May book-to-bill ratio remained positive for the sixth consecutive month and was especially strong for the flexible circuit segment of the industry. This reinforces our hope that sales will gain strength in the second half of this year.”

The Role of Domestic Production
IPC’s monthly survey of the North American PCB industry tracks bookings and shipments from U.S. and Canadian facilities, which provide indicators of regional demand. These numbers do not measure U.S. and Canadian PCB production. To track regional production trends, IPC asks survey participants for the percent of their reported shipments that were produced domestically (i.e., in the USA or Canada). In May 2012, 83 percent of total PCB shipments reported by survey participants were domestically produced. Domestic production accounted for 84 percent of rigid PCB and 80 percent of flexible circuit shipments in May by IPC’s survey participants. These numbers are significantly affected by the mix of companies in IPC’s survey sample, which change slightly in January, but are kept constant through the remainder of the year.
International Diary

13-16 Aug 2012
ICEPT - Electronic Packaging Technology
Shanghai, China
www.icept.org

5-7 Sep 2012
Semicon Taiwan
Taipei, Taiwan
www.semicon taiwan.org

11-13 Sept 2012
electronica India
Bangalore, India
www.electronica-india.com

11-13 Sept 2012
productronica India
Bangalore, India
www.electronica-india.com

9-11 Oct 2012
Semicon Europe
Dresden, Germany
www.semiconeuropa.org

16-17 Oct 2012
SMTA International
Orlando, FL, USA
www.smta.org
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  - Monitoring of pre and post-part placement
- Mixed Production of Different Boards/Independent Production at the Front and Rear/Non-stop Change-over of Device Types
- SMART Feeder
  - The world’s first Auto Splicing and Auto Loading functions

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**SM471**
Flexible High Speed Chip Shooter
- 75,000 CPH (Optimum)
- 2 Gantry x 70 Spindle/Head
- Applicable Parts: ø9mm to ø14mm (H12mm)
- Applicable PCB:
  - Max. 510L x 460(W)/Standard
  - Max. 610L x 440(W)/Option
- Electrically Driven High Speed and High Precision Feeder
- SMART Feeder
  - The world’s first Auto Splicing and Auto Loading functions

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**SM411N**
Dynamic & Flexible Chip Shooter
- Electrically Driven High Speed and High Precision Feeder
- Allows mixed use with an SM pneumatically driven feeder
- Placement Rate: 42,000 CPH (PC8580)
- Placement Accuracy: ±50μm ± 3x/4x
- Coverage PCB:
  - Max. 618mm (L) x 460mm (W) x 1 Lane
  - 618mm (L) x 250mm (W) x 1 Lane

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**SM421N**
Advanced Flexible Component Placer
- Electrically Driven High Speed and High Precision Feeder
- Allows mixed use with an SM pneumatically driven feeder
- Placement Rate: 21,000 CPH (PC9155)
  - SCP 15,000 CPH (PC9155)
  - QFP 5,000 CPH (PC9155)
- Coverage PCB:
  - Max. 744mm (L) x 450mm (W)
  - 618mm (L) x 450mm (W)

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**SMART Feeder**
- The world’s first Auto Splicing and Auto Loading functions
- Applicable to reels with a small quantity of parts
- Maximizes work convenience and actual productivity by automating the splicing process for part real replacement which has been performed by hand

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